INTEGRATED CIRCUIT LOGIC WITH SELF COMPENSATING BLOCK DELAYS

ABSTRACT OF THE INVENTION

An integrated circuit (IC) including at least one combinational logic path. The combinational logic path includes two types of logic blocks cells that compensate each other for fabrication parameter effects on cell transistors. The two types may be dense cells with field effect transistor (FET) gates on contacted pitch and isolated cells with FET gates on wider than contacted pitch. Dense cell delay changes from the FET gates being printed out of focus are offset by isolated cell delay changes.